FIG. 1

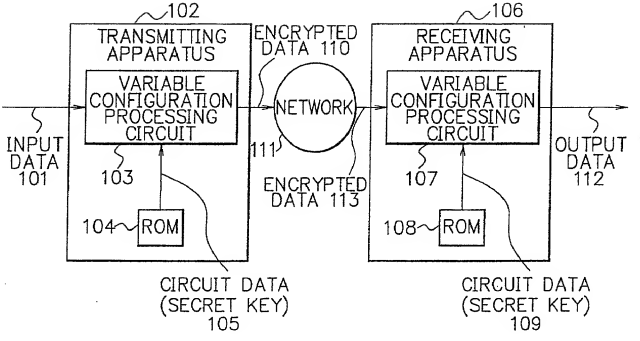

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FIG. 2

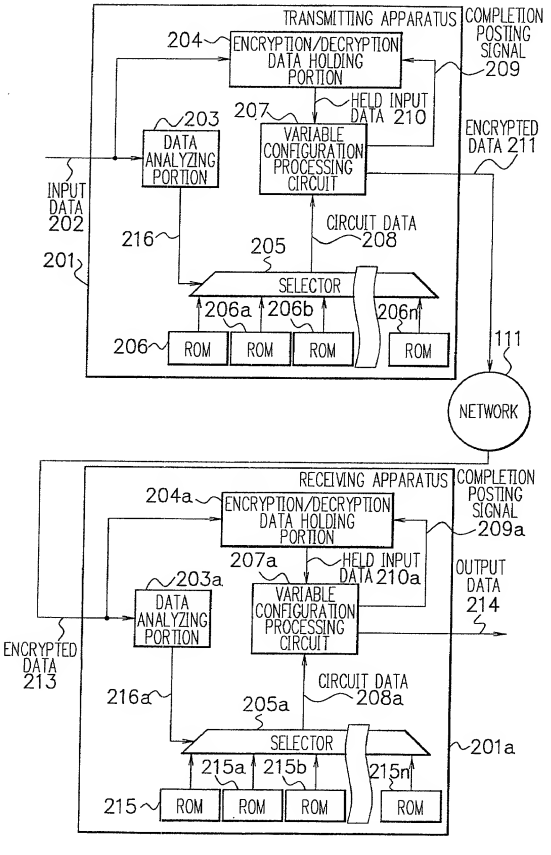
TRANSMITTING APPARATUS
204
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL 209
HELD INPUT DATA 210
207
203
DATA ANALYZING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
ENCRYPTED DATA 211
INPUT DATA 202
CIRCUIT DATA 208
216
205
201
SELECTOR
206a
206b
206n
206
ROM
ROM
ROM
ROM
111
NETWORK
RECEIVING APPARATUS
204a
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL 209a
207a
HELD INPUT DATA 210a
203a
DATA ANALYZING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
OUTPUT DATA 214
ENCRYPTED DATA 213
216a
CIRCUIT DATA 208a
205a
SELECTOR
201a
215a
215b
215n
215
ROM
ROM
ROM
ROM

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FIG. 3

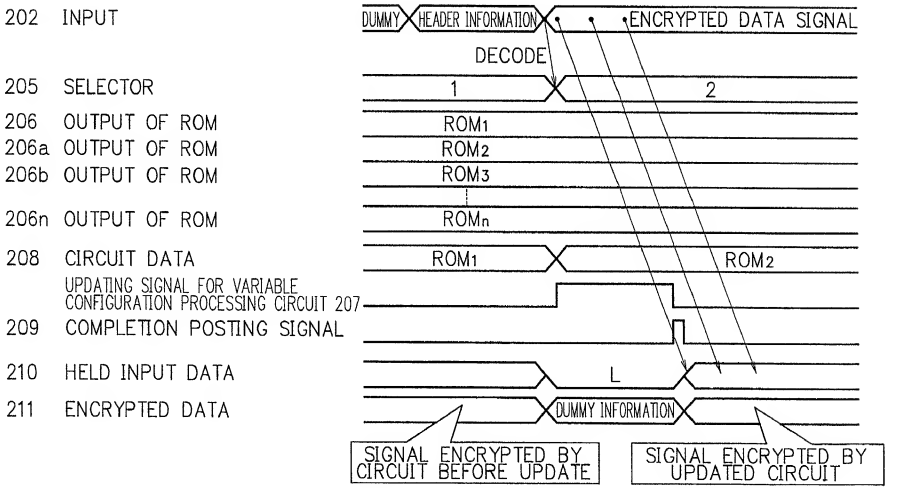

FIG. 4

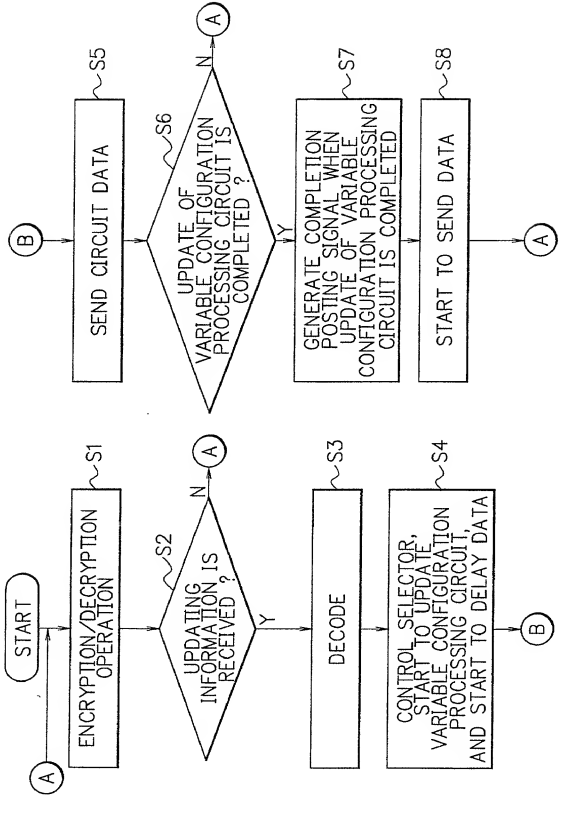
START
A
ENCRYPTION/DECRYPTION OPERATION
S1
UPDATING INFORMATION IS RECEIVED ?
S2
N
Y
DECODE
S3
CONTROL SELECTOR, START TO UPDATE VARIABLE CONFIGURATION PROCESSING CIRCUIT, AND START TO DELAY DATA
S4
B
SEND CIRCUIT DATA
S5
UPDATE OF VARIABLE CONFIGURATION PROCESSING CIRCUIT IS COMPLETED ?
S6
GENERATE COMPLETION POSTING SIGNAL WHEN UPDATE OF VARIABLE CONFIGURATION PROCESSING CIRCUIT IS COMPLETED
S7
START TO SEND DATA
S8

FIG. 5

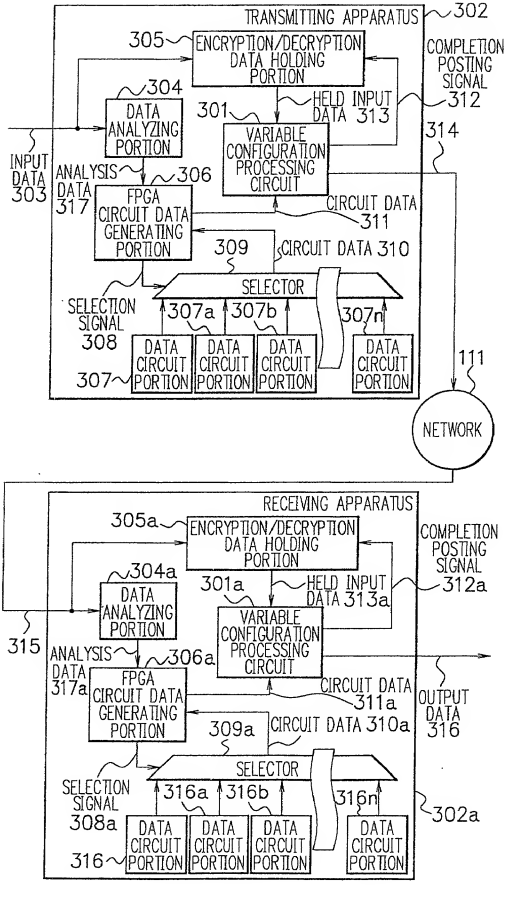
TRANSMITTING APPARATUS
302
305
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL
312
304
DATA ANALYZING PORTION
301
HELD INPUT DATA 313
314
VARIABLE CONFIGURATION PROCESSING CIRCUIT
INPUT DATA 303
ANALYSIS DATA 317
306
FPGA CIRCUIT DATA GENERATING PORTION
CIRCUIT DATA 311
309
CIRCUIT DATA 310
SELECTION SIGNAL 308
SELECTOR
307a
307b
307n
DATA CIRCUIT PORTION
307
111
NETWORK
RECEIVING APPARATUS
305a
ENCRYPTION/DECRYPTION DATA HOLDING PORTION
COMPLETION POSTING SIGNAL
312a
304a
301a
HELD INPUT DATA 313a
DATA ANALYZING PORTION
VARIABLE CONFIGURATION PROCESSING CIRCUIT
315
ANALYSIS DATA 317a
306a
FPGA CIRCUIT DATA GENERATING PORTION
CIRCUIT DATA 311a
OUTPUT DATA 316
309a
CIRCUIT DATA 310a
SELECTION SIGNAL 308a
SELECTOR
316a
316b
316n
302a
DATA CIRCUIT PORTION
316

FIG. 6

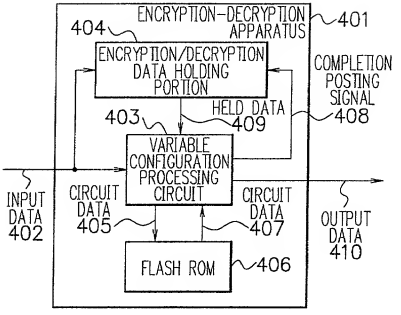

FIG. 7

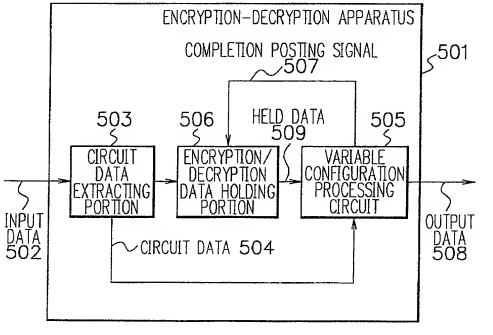

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FIG. 8

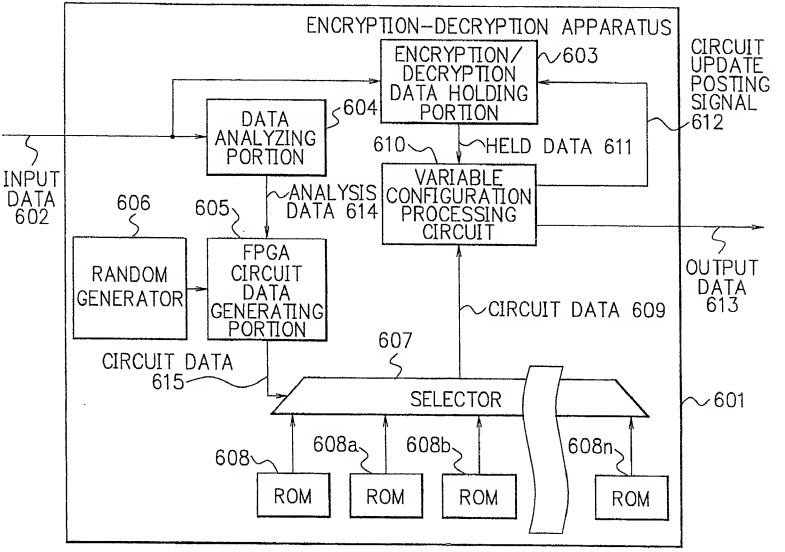

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FIG. 9

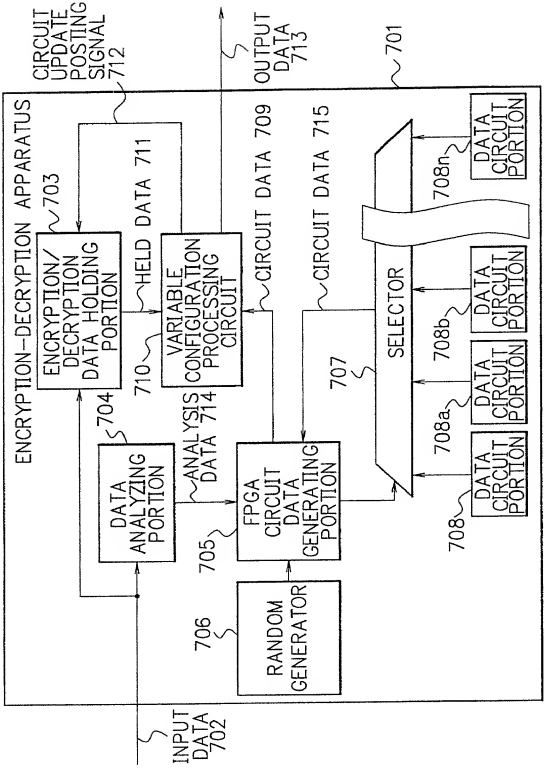

FIG. 10

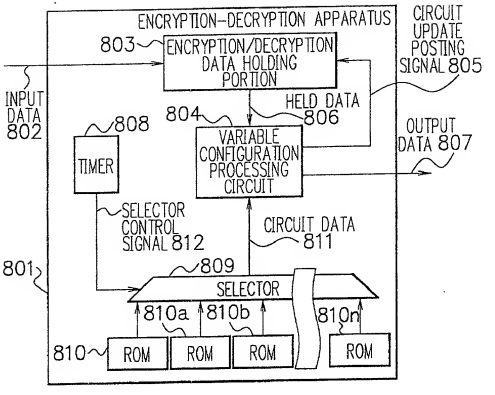

FIG. 11

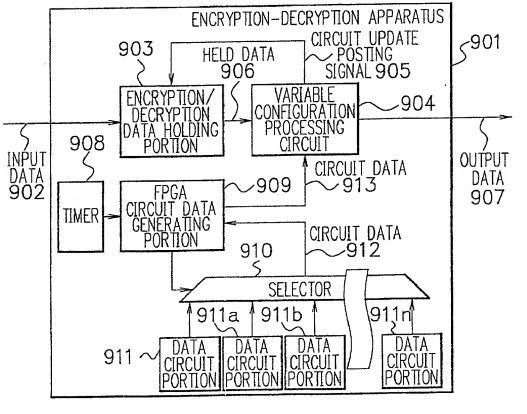

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FIG. 12

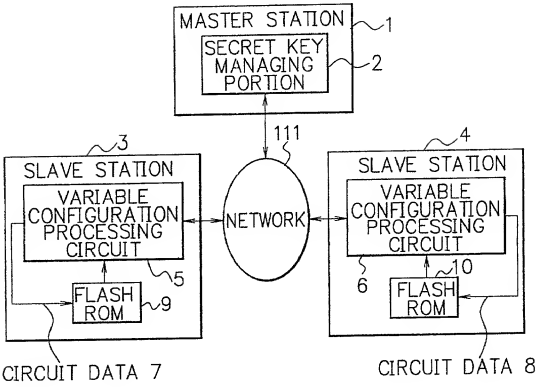
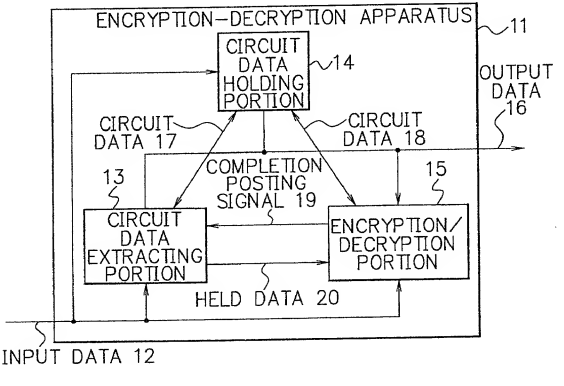


FIG. 13



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